PECOAT

Power Electronics Coatings

State of the art – Background

Power electronic converters used in aircraft have previously been used at reasonably low voltages which have not been associated with a significant risk of electrical discharge. Items such as circuit boards are designed in accordance with standards such as IPC2221A but this is often seen as conservative. Given the drive to the more electric aircraft and the need to increase power density of the electrical sub-systems, power electronic converters are now at increased risk of electrical discharge given the increase in voltage and are under increased pressure to remain as compact and light weight as possible. This project intended to identify a coating that could be applied to power electronic converter components to reduce the risk of electrical discharge associated with the use of high voltages and will identify suitable techniques for integrating the application of this coating within a manufacturing environment. The project was focused on the protection of power electronic systems operating at high voltage within an open-box environment, this meaning the pressure and temperature will vary within the box as a function of operating altitude. There is also a significant risk from high levels of humidity and condensation when operating within an open-box environment.

The use of any high voltage system on an aircraft introduces a risk of damage from electrical discharge. This risk is exacerbated by low pressure, humid and variable temperature environments. Electrical discharge can be subdivided into three categories; disruptive discharge, partial discharge and tracking. The risk from all of these must be considered in the design of any insulation system. As aerospace power systems move to higher voltages, these forms of discharge must be considered in their design. At present, there is little guidance in this area and SAE have recognised this through the development of an Aerospace Information Report 'High Voltage Design Guidelines for Aerospace Systems'.

The first electrical discharge type that must be considered in the design of any higher voltage system is disruptive discharge. This results in a flow of fault current between two electrodes and would usually necessitate the operation of some form of power system protection to clear the fault. An example of where a disruptive discharge could occur is in an air gap between two un-insulated electrodes (for example, uncoated leads on a PCB) should these not be kept a sufficient distance apart. Disruptive discharges can also take place through liquid and solid insulation if the insulation levels are not thick enough although the breakdown processes are governed by the form of insulation used and are not usually sensitive to pressure unless cavities or voids are present. The dielectric strength of solid and liquid insulation is usually magnitudes higher than air.

Partial discharges are small discharges that do not completely bridge a gap between two electrodes. Partial discharges in cable insulation voids, discharges between adjacent insulating conductors and similar modes will take the form of a discharge in air. The presence of partial discharge can reduce the service life of a system by degrading insulation. Repetitive discharge events can cause irreversible mechanical and chemical deterioration of the insulating material. Damage can be caused by the energy dissipated by high energy electrons or ions, ultraviolet light from the discharges and ozone attacking the insulation. The chemical transformation of the dielectric can also tend to increase the electrical conductivity of any surrounding dielectric material and can increase the electrical stress in the remaining unaffected insulation leading to an acceleration of the breakdown process.

Tracking can occur at any voltage and is typically connected with the presence of a liquid contaminant on an insulation surface across which an electric field is present. Tracking can also occur across dry surfaces although the voltages required are generally much higher. For the more common wet tracking, when a liquid layer is deposited between two electrodes, a current will flow in the liquid. Heating of this liquid layer will lead to evaporation. This will often take place in the middle of the gap away from the electrodes which stabilise the temperature of the nearby liquid. As the liquid evaporates, a spark will develop across the new dry band. The spark, if energetic enough, can damage the underlying insulation. Should carbonaceous deposits develop, this can accelerate further damage owing to the degradation of the 'healthy' insulation within the gap. The severity of the damage will depend on the voltage and current of the arc along with the characteristics of the material itself.

Some design standards exist to ensure dielectric systems are designed with appropriate creepage and clearance distances. IEC 60664 provides

guidelines valid for altitudes up to 2000 m for dimensioning clearance distances (to avoid a disruptive discharge) and creepage distances along surfaces (to prevent tracking). The guidelines are based on empirical data and are not applicable to equipment installed in lower pressure environments. In a similar way IPC2221A provides the information on the distances between tracks on printed circuit boards but does this for all altitudes. Aerospace Standard AS50881 provides guidance for choosing conductor and insulation sizes for aerospace wiring. Conductor size is based on an analysis of the required current carrying capability and takes the impact of altitude and the use of conductor bundles into account. Insulation size is determined by examining the required operating voltage, the insulation selected being thick enough to withstand partial discharges.

The aerospace environment has a significant impact on all of these forms of electrical discharge and the measures that are required to ensure their elimination. The air pressure is the key factor that changes significantly from that observed in a ground based environment. This leads to a higher risk of disruptive and partial discharge as the air density lowers – at 15,000 m clearances must be increased in size by a factor of around 14.5. Tracking is also affected by pressure owing to the change in boiling point of any liquid contaminant sitting on the surface of insulation. In the correct conditions, a 4 mm gap can only withstand a voltage of 50 V before tracking damage takes place. There is therefore a clear risk of using uncoated electronics in an aerospace environment where humidity leads to an increased risk of tracking although the exact nature of this relationship is unclear given the different ways in which humidity and air pressure vary as a function of altitude. Low pressure also increases the risk of damage from tracking but also increases the risk of disruptive discharges and partial discharges.

Coatings applied to high voltage equipment can reduce the risk of electrical discharges but also introduce another set of risks. The probability of disruptive discharges is reduced as electrodes are coated and gaps in which an arc can bridge a gap between two electrodes are eliminated. Tracking damage is also minimised through the coating imposing a limitation on the level of current that can flow through any liquid contaminant or resulting arc. However, coatings must be capable of withstanding the dielectric stress that they see when placed between two electrodes and in any situation where contamination is present on the circuit board surface. An ideal coating would be homogenous and defect free, if voids are present it could lead to partial discharge or dielectric failure of the interface between the circuit board and the coating.

Conformal coatings based on polymer films have been applied commercially onto electronic circuit boards. However, they might not be suitable for use in the low pressure environment of high voltage power electronics given the relative poor performance of such coatings when exposed to tracking / partial discharge. In contrast, physically robust, relatively low cost and light weight polymer composite with microfillers based insulators which are capable of lasting over 20 years at the highest voltages have been used in the electricity network. However, thus far, such polymer composites tend to be fabricated and used in the bulk form.

Fabricating a new material for PCB coating in an aerospace environment is therefore likely to be challenging and any move to do so must be driven by a clear understanding of the existing margins of PCB coatings in an open box environment

Objectives

This project examined the options for the deployment of novel and cost-effective coatings to be placed onto the printed circuit boards and power electronic components that may require protection in open box power electronics. The focus was on developing:

- A coating type that can withstand the aerospace environment
- A coating that when applied to open box power electronics will inherently reduce the risk of electrical discharge (i.e. discharges that take place at the high levels of electric field associated with the use of higher voltages)
- A coating that is straightforward to apply (ideally using techniques identical to those in present manufacturing)
- A coating that can withstand damage from electrical discharges should a localised defect occur which allows these to take place

Description of work and Results

Work packages 1 and 2 focussed on an experimental assessment of the range of candidate coatings and possible failure mechanisms. A wide range of experimental testing was designed to simulate worst case conditions, and included:

- Thermal aging: Accelerated aging of coatings as a result of exposure to high temperatures conducive to increased chemical reaction rates.
- Thermal cycling: Subjection to rapid temperature changes resulting in mechanical stressing of coatings, possibly leading to cracking and susceptibility to water ingress
- Humidity (and submersion): Exposure of coatings to high humidity environments and also submersion of boards into salt water solutions to examine water ingress
- Tracking: Surface arcing between energised tracks as surface pollution evaporates, leading to erosion and carbonised tracks in the coating and increased risk of disruptive discharge
- Partial discharge (PD): Corona discharge on or within the coating leading to accelerated aging and degradation from the UV, high energy electrons, and chemical changes
- Breakdown: Subjecting boards to sufficiently high voltages that breakdown and failure occurs, to identify the voltage limits

This initial testing was conducted on relatively simple coatings consisting of a polymer absent of any micro- or nano-fillers. Polymers examined included polyurethane, acrylic (both sprayed and dipped application techniques), parylene, and silicone. Testing concluded that thermal cycling, thermal aging, and humidity had little influence on the resulting breakdown voltages relative to unaged samples. Tracking was also unlikely to occur owing to the small gap spacings being tested leading instead to full breakdown through the polymer coating. Partial discharge was observed to have the most substantial aging and degrading effect on all coatings. As such, partial discharge was considered to be the principal focus of subsequent testing. Nevertheless, the breakdown voltages at track spacings comparable to those at the lower end specified in standards (IPC 2221A, IEC 60664) showed that the polymer coatings used, particularly silicone, were performing considerably above specification. This also highlighted the level of conservatism adopted by the standards. As such, the decision to focus subsequent investigations into more complex coatings was considered unnecessary. Coatings were down-selected to parylene, acrylic, and silicone, going forward.

Subsequent testing in work package 3 focussed initially on the onset and influence of partial discharge on the down-selected coatings. Testing was conducted to measure the partial discharge inception voltage (PDIV) for coated boards as a function of pressure. A pressure dependence was observed. Subsequent finite element analysis (FEA) was performed to model the fields associated with the observed PDIV to help estimate the PD-free operating voltages on boards as a function of coating thickness and track separation.

Additionally, tests were conducted to quantify the magnitude and rate of PD damage on the range of down-selected coatings as a function of applied voltage above PDIV. Amongst the results observed, it was concluded that partial discharge self-generated by the board, rather than being externally applied, was highly likely to be a surface based phenomenon rather than occurring within the bulk, e.g. in voids. The pressure dependence, the surface-only damage, and the electric field dependence despite different coating thicknesses, supported this conclusion. This work ultimately led to recommendations to industry partners for track spacings and candidate board designs to subsequently test using the coating identified as the optimal choice.

In work package 4, new boards were manufactured, designed to recommendations based on results from work package 3, and coated. Some boards also had mounted components from an external supplier to help test coating application quality. Only a few of these boards were initially tested for PDIV, and first results showed that the reduced spacings indeed met and often considerably exceeded the recommendations. However, it was observed that boards with tall components had thinner coatings on corners, and this was reducing the relative breakdown strength. In addition, voids were present between the taller components, although no evidence was found that their presence affected PDIV or reduced breakdown strength. A revised coating application technique was developed and employed to eliminate these two factors before subsequent testing on the rest of the boards. The technique also ensured optimal and homogeneous coating thickness and was recommended to industry partners.

Following changes to coating thickness from this revised coating technique, updated recommendations on track spacings were provided to industry partners. Full testing at low pressure of all boards with the revised coating technique led to the conclusion that all boards surpassed our recommendations with substantial safety factors.

The aim of work package 5 was to confirm the coating techniques and recommendations that were successfully applied in work packages 3 and 4, would transfer to full-sized populated boards more akin to those found in service. Component mounted boards with reduced track spacing were provided by the industry partner and coated to specification from earlier recommendations. Boards were then tested to the maximum voltage rating of components at low pressure and low ambient temperature. After testing, conductive pollution was applied to four locations on the circuit boards identified to be subjected to the highest electrical stress and testing was repeated. No partial discharge was observed with or without conductive pollution, confirming such boards remain PD free with the new recommendations.

a) Timeline & main milestones

End of month 13: Coating choice / application technique down-selection
End of month 21: 12 month review
End of month 21: Test designs reported and test rigs designed
End of month 32: Open Box power converter coated
End of month 33: All testing complete
End of month 33: Project closeout

b) Environmental benefits

c) Maturity of works performed

The project has several potential commercial impacts for the industrial partner. The formulation of new design guidelines for the determination of track spacings on printed circuit boards and revised coating techniques will allow the industrial partner to modify their production processes and to produce circuit boards of reduced size. The design guidelines will also allow the industrial partner to design circuit boards that are free of partial discharge at the nominal operating voltage. The use of low cost coatings of optimal thickness will allow the power electronics to operate with increased power density, and being open to the aerospace environment will allow further weight savings through the removal of hermetically sealed enclosures currently used for the protection of power electronics in aircraft. The size reduction of electronics boards, the removal of heavy enclosures, and the use of low cost coating materials, will potentially be beneficial to aircraft manufacturers and airlines through savings derived from reduction in fuel consumption and carbon emissions.

The findings of the project have been disseminated to the wider aerospace and electrical insulation communities. Results regarding the ageing of silicone coatings due to partial discharge were presented at the IEEE Electrical Insulation Conference in Seattle, Washington, in June 2015 and at a special seminar session at Rolls Royce, UK in February 2015. An article on the ageing of coatings titled "Degradation of Conformal Coatings on Printed Circuit Boards due to Partial Discharge" has recently been accepted for publication in the IEEE Transactions on Dielectrics and Electrical Insulation. It is also anticipated that the findings regarding reduced track spacings and ageing of a range of coating types could influence future aerospace standards from organisations such as the SAE, IPC, or IEC.

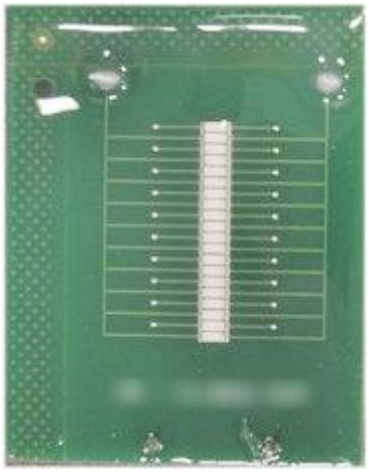

Image of optimally coated test sample circuit board. The board has a high quality, void-free, uniformly applied silicone coating providing good edge coverage.

Project Summary

Acronym : PECOAT

Name of proposal: Novel Coating Systems For Power Electronics In Aerospace Environments

Technical domain: SGO

Involved ITD

Grant Agreement: 307309

Instrument: Clean Sky JU

Total Cost: 484,233.80

Clean Sky contribution: 363,175.35

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